

Preface

From the beginning of its development until the present day, microelectronic technology has made continuous and unstoppable advances in the miniaturization of the basic components of integrated circuits. This miniaturization has had two fundamental consequences. First of all, the capacity to implement extremely complex systems within a single chip. Secondly, an increasingly higher operation speed in the circuits, more and more comparable to the propagation speed of the electrical signals passing through the conductors of the chip.

In order to achieve such highly complex system designs, the designer needs to use CAD tools for synthesis as well as for verification. The latter are meant to check that each design description meets the behavioural specifications.

An aspect which is often overlooked is that the tools or, rather, the precision of the results obtained with those tools, is very sensitive to technological variations. In particular, verification tools lose precision because the behavioural models of the devices they implement lose validity with technological evolution. In order to avoid this loss of precision in the results it is necessary to carry out a constant update of the tools by analysing and improving behavioural models.

The timing behaviour of digital circuits is undoubtedly one of those with the greatest sensitivity to technological variations. This, along with the fact that the aim is to achieve a maximum circuit operation speed, implies a constant scientific need for analysis and improvement of the timing behavioural models which allow the tools to obtain results which are sufficiently reliable for the designer.

This book focuses on this line of work. More specifically, it deals with the modelling of the timing behaviour of logic devices (especially of logic gates) and the simulation tools at the logic level which allow for the timing analysis of large digital circuits. Precision in the timing analysis at gate level is of the utmost importance for several reasons. On the one hand, it is important from the point of view of the designer, who normally follows a Top-Down methodology, because it is at the gate level where timing behaviour is first encountered physically since at a previous level only clock cycles are modelled. In addition, it is important because the gate level is the last one common to practically all forms of implementation: Full-custom, Standard Cell Semi-Custom, and even FPGAs. On the other hand, from the point of view of timing simulation applications, there are several reasons: 1) it is essential not only for verifying the correctness of the design at the timing level but also for characterizing the performances, an aspect which may in turn be applied to the redesign of those parts of the circuit which do not offer the desired performance; 2) analysis and treatment of collisions and glitches, with applications in the study of asynchronous interactions or desynchronized signals and in the prevention of undesired behaviour such as metastability; 3) measuring switching activity, with direct application to the analysis of consumption and noise generation in mixed analog-digital circuits.

We have structured the book into eight chapters. The first two chapters are general while subsequent ones deal with the specific results of our research team in this line of work, both in delay modelling as well as in the implementation of simulation tools and their application to the verification of the designs.

The first chapter is devoted to the fundamental aspects of timing simulation. Specifically, various techniques are analysed which were developed so that a designer may carry out the timing simulation of a design. Thus, simulation is analysed at the electrical level, undoubtedly the one with the most precise results, which, in addition, serves as a reference for measuring the quality of the other types of timing simulation. However, the excessive use of computer resources (CPU time, memory, *etc.*) makes it completely nonviable, especially when aiming to simulate the behaviour of systems of considerable complexity. In this chapter other alternatives for the timing simulation are also analysed, such as simulation at the

transistor level or at the logic gate level. Advantages and disadvantages are described along with a brief description of the event-driven simulation technique employed in these kinds of timing simulations.

In Chapter 2 we focus on the logic timing simulation at the gate level and, more specifically, on the delay models which are implemented in the simulators. A review of the delay models is carried out, starting with the zero delay model, that is, without considering any specific timing behavioural effect, followed by a presentation of successive models of increasingly higher complexity. Thus, models are presented which include static effects as well as dynamic effects which affect the propagation delay.

The so-called inertial and degradation effects are introduced in Chapter 3. The behaviour of the gates with respect to these effects is studied and the so-called Degradation Delay Model (DDM) is presented. By applying the DDM, a study is carried out on the importance of the degradation effect, concluding that specially in very high speed designs, it is fundamental to take it into account in order to achieve a correct verification of the designs. On the other hand, a detailed analysis is given of the inertial effect and the so-called inertial delay, a model widely used to include this effect within the logic simulation. In this chapter it is shown how the Inertial Delay can produce significant errors in the simulation results and an alternative algorithm is proposed to include said effect within the logic simulation, resolving the problem.

Chapters 4 and 5 are devoted fully to developing the DDM. Specifically, Chapter 4 presents a very exhaustive characterization of the typical DDM parameters with respect to the technological parameters of a CMOS inverter.

The step from modelling a gate with a single entry such as the inverter to modelling gates with several entries is not a trivial one. Indeed, the model may be realized by obtaining an equivalent inverter, but also by applying the same DDM concept to the different gate entries. In Chapter 5 an extension of the model to the complex CMOS gates is made.

The next two chapters are devoted to presenting the characteristics of a simulation tool called HALOTIS (High Accuracy LOGic Timing Simulator), which implements the DDM model along with the results obtained. Chapter 6 is devoted to presenting the general structure of the tool along

with the basic characteristics of the simulation engine and the delay model interface.

Chapter 7 is in turn devoted to presenting the results of HALOTIS simulation using two different behavioural models, the DDM and the CDM (Conventional Delay Model, which differs from the DDM in that it does not include the degradation effect). These results are moreover compared with those obtained by means of electrical simulation. Three types of results are presented which we consider significant: simulation of pulse propagation/pulse trains through a chain of gates; calculation of the operating frequency of a three-inverter ring oscillator; and the simulation of the metastable behaviour in several latches designed at the logic gate level. The results clearly show that there is quite a significant increase in the precision of the results when the degradation effect is included in the logic simulation.

Lastly, in Chapter 8 of this book a detailed analysis of the switching activity within the digital circuits is carried out with different types of timing simulators. The switching activity is a direct measurement of the average number of changes in the nodes of a circuit. It is a fundamental parameter for measuring the consumption and the switching noise in digital circuits. Actually, most tools for estimating the consumption of energy in digital circuits employ switching activity as a fundamental parameter. In this chapter, on the one hand, a detailed quantitative study on the ISCAS85 benchmark circuits is carried out, demonstrating that the activity due to glitches can become as significant as the functional activity inherent to the circuit (the one due to the operation of the circuit). The numerical values here presented show the great importance of treating glitches when measuring switching activity. On the other hand, the measurements of this parameter obtained with logic simulators are presented, showing that commercial simulators can make serious errors, whereas HALOTIS (using DDM) increases precision significantly.